Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTION:**

1. **IN1**
2. **D1**
3. **S1**
4. **V-**
5. **GND**
6. **S4**
7. **D4**
8. **IN4**
9. **IN3**
10. **D3**
11. **S3**
12. **VL**
13. **V+**
14. **S2**
15. **D2**
16. **IN2**

**.080”**

**2 1 16 15**

**3 14**

**4 13**

**5 12**

**6 11**

**7 8 9 10**

**.097”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” x .004” min.**

**Backside Potential:**

**Mask Ref: AG38Y**

**APPROVED BY: DK DIE SIZE .080” X .097” DATE: 8/30/22**

**MFG: MAXIM THICKNESS .017” P/N: DG412**

**DG 10.1.2**

#### Rev B, 7/19/02